APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

CASCADED PHASE-LOCKED LOOPS

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CASCADED PHASE-LOCKED LOOPS

BACKGROUND OF THE INVENTION

1.   FIELD OF THE INVENTION

5   Embodiments of the present invention relate to the field of circuit design. More

specifically, embodiments of the present invention relates to a cascaded PLL

arrangement.

2.   BACKGROUND INFORMATION

10   Over the years, ongoing advancements in the field of microprocessor design and

fabrication have facilitated the continued increase in microprocessor clock frequencies.

High frequency microprocessor core clocks are typically synthesized from existing,

lower frequency external reference clocks such as a bus clock. In the past, it was fairly

simple to achieve a desired core frequency using PLLs as microprocessor core-to-bus

15   frequency ratios were relatively low. Nowadays however, in order to generate the multi-

Gigahertz microprocessor core frequencies that are typical, a large PLL synthesis factor

is required. Unfortunately, as PLL synthesis factors increase, the circuit area required

to implement the PLLs also increases.

In the past, microprocessor core clock signals and microprocessor I/O clock

20   signals have been generated by two PLLs disposed in a parallel arrangement with

respect to one another. Figure 1, for example, illustrates a prior art dual-PLL

arrangement where the PLLs are arranged in a parallel configuration. As shown, the

external reference clock, xclk, is routed to both I/O PLL 104 and Core PLL 114 to

generate Data clock 109 and Core clock 119 respectively. In order to generate a Core

clock signal having a frequency that is N times greater than the frequency of xclk, the

damping factor (which is a measure of PLL stability) of Core PLL 114 is reduced by a

factor equivalent to the square root of N. One problem with this arrangement, however,

5   is that a lower damping factor can also cause jitter amplification in certain phase-

modulation frequencies. Additionally, any phase noise associated with xclk will be

propagated through to Core clock 119 with only one level of filtering. Moreover, since

the bandwidth of Core PLL 114 is very high, the effectiveness of the phase noise

filtering is reduced.

10   Another problem associated with the parallel PLL configuration illustrated in

Figure 1 involves the synchronous transfers between timing domains. Because the

parallel PLLs do not track each other very closely, a timing margin is often required to

facilitate synchronous data transfer from one timing domain to another in a deterministic

manner. Unfortunately, however, such timing margins typically shrink as

15   microprocessor core operating frequencies increase potentially resulting in clock

instability.

BRIEF DESCRIPTION OF DRAWINGS

The present invention will be described by way of exemplary embodiments, but not limitations, illustrated in the accompanying drawings in which like references denote similar elements, and in which:

5　　　　Figure 1 illustrates a first and second PLLs disposed in a parallel relationship according to the prior art;

Figure 2 illustrates clock generation circuitry utilizing cascaded PLLs in accordance with one embodiment of the invention;

Figure 3 illustrates an example PLL suitable for cascading with one or more

10　　additional PLLs in accordance with one embodiment of the invention; and

Figure 4 illustrates one embodiment of a microprocessor including the cascaded PLL clock generation circuitry of Figure 2.

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DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

A method and apparatus for generating clock frequencies using cascaded phase-locked loops (PLL) is described. In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the present

5   invention. However, those skilled in the art will understand that the present invention may be practiced without these specific details, that the present invention is not limited to the depicted embodiments, and that the present invention may be practiced in a variety of alternative embodiments. In other instances, well known methods, procedures, components, and circuits have not been described in detail.

10   Various operations will be described as multiple discrete steps performed in turn in a manner that is helpful for understanding the present invention. However, the order of description should not be construed as to imply that these operations are necessarily performed in the order they are presented, nor even order dependent.

Reference throughout this specification to "one embodiment" or "an embodiment"

15   means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment or invention. Furthermore, the particular features, structures, or

20   characteristics may be combined in any suitable manner in one or more embodiments. Lastly, the terms "comprising", "including", "having", and the like, as used in the present application, are intended to be synonymous.

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Figure 2 illustrates clock generation circuitry utilizing cascaded PLLs in accordance with one embodiment of the invention. As shown, clock generation circuitry 200 includes I/O PLL 202 coupled to core PLL 212 in a cascaded manner, as shown. In particular, I/O PLL 202 receives reference signal 201, and in turn generates data clock

5   signal 203. Data clock signal 203, or a divided down version of data clock signal 203, is then used as a reference clock signal for core PLL 212 which in turn generates core clock 213. In one embodiment, data clock signal 203 is used for source synchronous communication between a microprocessor and its memory subsystem, whereas core clock 213 is utilized by the microprocessor core.

10   In addition to I/O PLL 202 and core PLL 212, clock generation circuitry 200 further includes feedback frequency dividers 204, 206 and 214. Each of feedback frequency dividers 204, 206 and 214 represent circuitry to divide the frequency of an input signal by an integer value to produce an output signal having a reduced or "divided-down" frequency as compared to an input signal. More specifically, in the illustrated

15   embodiment, feedback frequency divider 204 generates feedback signal 205 based upon data clock signal 203, feedback frequency divider 206 generates reference signal 209 based upon data clock signal 203, and feedback frequency divider 214 generates reference signal 215 based upon core clock signal 213. In one embodiment, one or more of feedback frequency dividers 204, 206 and 214 are selectively programmable so

20   as to divide the frequency of an input signal by a selected factor. In one embodiment, feedback frequency divider 206 may be selectively programmed to divide the frequency of data clock signal 203 by a factor of 4, 2 or 1. Similarly, in one embodiment, feedback frequency divider 214 may be programmed to divide the frequency of core clock signal

213 by an integer value selected from a group of integer values including a low integer

value, and a high integer value that is less than two times the low integer value. In one

embodiment, feedback frequency divider 214 may be programmed to divide the

frequency of core clock signal 213 by an integer value that is greater than or equal to 12

5   and less than or equal to 23. For example, if feedback frequency divider 206 is set to

divide data clock signal 203 by 1, 2 or 4, the effective synthesis factor range of clock

generation circuitry 200 would be 12-23, 24-46 and 48-92, respectively.

By selecting a higher multiplied input reference frequency for the Core PLL, its

output frequency can be ratcheted up to reach a higher synthesis multiplication factor.

10   Because the Core PLL's ratio range is small, its damping factor fits in a tight design

range, and the filter capacitor required to stabilize the Core PLL can be minimized.

Since the implementation area of a PLL is largely dependent upon the total capacitance

of the PLL, a cascaded PLL arrangement facilitates leveraging a wide synthesis range

while reducing the overall PLL implementation size. Moreover, the cascaded

15   arrangement of I/O PLL 202 and core PLL 212 provides an additional level of filtering of

external reference clock phase noise not available in single PLL implementations.

Figure 3 illustrates an example PLL suitable for cascading with one or more

additional PLLs in accordance with one embodiment of the invention. As shown, PLL

20   300, includes phase-frequency detector (PFD) 322 for monitoring a phase difference

between a reference signal 324 and a feedback signal 326 (in the form of a frequency

divided output signal of a voltage-controlled oscillator (VCO 328). The PFD 322

generates an UP control signal 330 and a DOWN control signal 332 to cause a charge

pump 334 to respectively charge and discharge a loop filter 336. The loop control

voltage 338 developed across the loop filter 336 determines the output frequency of the

VCO 328. Furthermore, the UP and DOWN control signals 330, 332 that drive the

charge pump 334 set the proper loop filter control voltage 338 at the input of the VCO

5   to maintain a minimal phase error between the input signals applied to the PFD 322.

During lock acquisition, the PFD attempts to correct for frequency differences

and/or phase misalignments between the reference and feedback clocks 324, 326.

The correction comes in the form of the UP/DOWN control signals 330, 332 whose

pulse-widths are proportional to the frequency and/or phase error between the two input

10   signals. The pulse width of the UP/DOWN control signals 330, 332 informs the charge-

pump as to how much current to source or sink from loop filter capacitors.

Figure 4 illustrates one embodiment of a microprocessor including the cascaded

PLL clock generation circuitry of Figure 2. In the illustrated embodiment of Figure 4,

15   microprocessor 475 includes I/O PLL 202 and core PLL 212 coupled together in a

cascaded manner as shown. In one embodiment, the data clock signal generated from

I/O PLL 202 is used by I/O block 450 of microprocessor 475 to facilitate data and

address latching within a first time domain, while the core clock signal generated from

core PLL 212 is used by core block 460 of microprocessor 475 to facilitate latching in a

20   second time domain. However, because the cascaded PLL arrangement of figures 2

and 4 facilitates tight tracking between the two clock domains, a reduced timing margin

between the domains may be achieved. In one embodiment, the loop bandwidth of core

PLL 212 is at least three times greater than the loop bandwidth of I/O PLL 202.

Although it may not be readily apparent from Figure 4, signal path 411 which provides reference signal 409 to PLL 212, and signal path 415 which provides feedback signal 415 to PLL 212 may be associated with long distributions. In one embodiment, to reduce the impact of global supply noise that may occur due to the long signal

5   distributions, signal path 411 and signal path 415 are equalized in length so as to provide first-order common mode tracking.

Epilog

While the present invention has been described in terms of the above-illustrated

10   embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described. For example, the PLL of Figure 2 may be used in one or more chipsets in addition to the microprocessor of Figure 4. The present invention can be practiced with modification and alteration within the spirit and scope of the appended claims. Thus, the description is to be regarded as illustrative instead of restrictive on the

15   present invention.